数据资料

精确的死区時間控制的桥型控制器

ISL6745是成本低、双端控制器。主要应用于全桥和半桥型拓扑结构的电源和线调节的总线变换器。器件的主要特点是精确的开关频率控制、可调软启动、和过流关断保护。另外，ISL6745 可精确地调整MOSFET不交迭的死区時間低至35ns，允許电源设计师优化开环总线变换器的效率。ISL6745 还包括电压控制输入适合于闭环PWM控制和线压前馈控制。

ISL6745的低启动和运作电流特点，使其在AC-DC和DC-DC应用容易地偏压。

这先进的BiCMOS设计特点是可调开关频率高至1MHz，1A FET驱动器，和非常低的传输延迟适合于过流快反应。

定购资料

零件号码	温度范围(°C)	包装	包装图号 #
ISL6745AU	-40 to 105	10 Ld MSOP	M10.118
ISL6745AUZ (See Note)	-40 to 105	10 Ld MSOP (Pb-free)	M10.118

Add -T suffix to part number for tape and reel packaging

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

主要特点

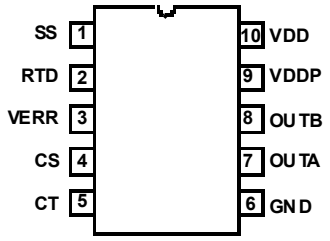
- 精确的占空比和死区時間控制
- 100µA 启动电流
- 可调延迟过流关断和重新启动
- 可调振荡器频率高至 2MHz
- 1A MOSFET 门极驱动器
- 可调软启动
- 内部过热保护
- 控制到输出的延迟是 35ns
- 体积小和极少的外部元件
- 输入欠压保护
- 不含 Pb 的包装

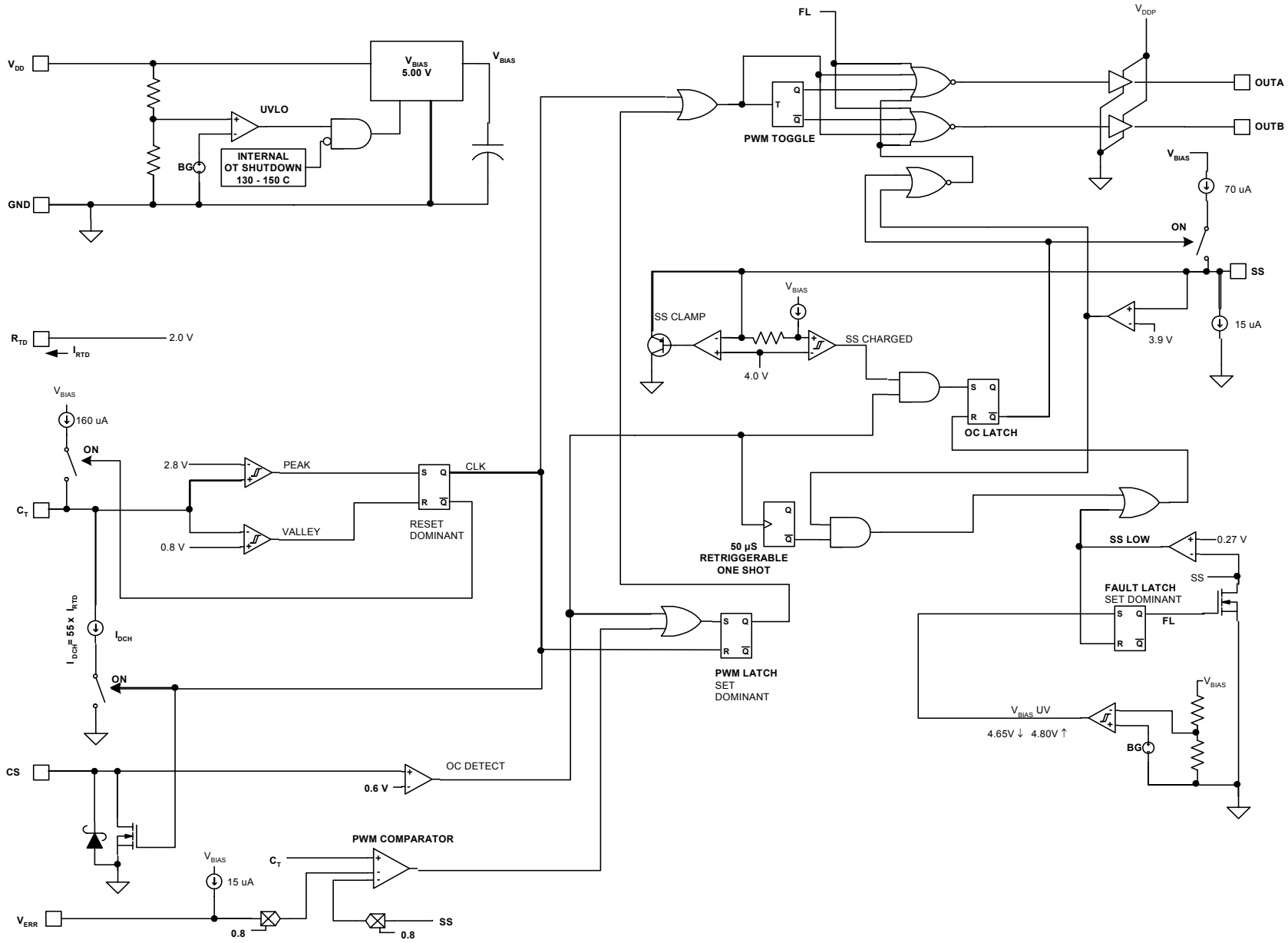
应用

- 半桥和全桥型拓扑结构的变换器
- 线调节的总线变换器
- AC-DC 电源
- 通信、信息和档案服务器的电源

插脚引线 (顶视图)

ISL6745 (MSOP)





ISL6745 内部电路结构

额定值

Supply Voltage, V_{DD} ----------GND-0.3V to +20V
OUTA, OUTB ---------- GND -0.3V to V_{DD}
Signal Pins---------- GND-0.3V to 5V
Peak GATE Current---------- 1A
ESD Classification
Human Body Model (Per JEDEC22 std. Method A114-B)---Class 2
Machine Model (Per JEDEC22 std. Method A115-A)---------Class A

运行条件

Supply Voltage Range (Typical) ----------9-16VDC
Temperature Range
ISL6745AU---------- -40°C to 105°C

热性能的资料

Thermal Resistance (Typical, Note 1)---------- θ_{JA} (°C/W)
10 Lead MSOP ---------- 128
Maximum Junction Temperature ---------- -55°C to 150°C
Maximum Storage Temperature Range --65°C to 150°C
Maximum Lead Temperature (Soldering 10s)------300°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

1) θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

2) All voltages are to be measured with respect to GND, unless otherwise specified.

Electrical Specifications

电气规范 Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block Diagram and Typical Application Schematic. 9V<V_{DD}<16V, R_{TD}= 51.1KΩ, C_T = 470pF, T_A = -40°C to 105°C (Note 4), Typical values are at T_A= 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE					
Start-Up Current, I_{DD}	V_{DD}< START Threshold	-	-	175	µA
Operating Current, I_{DD}	$C_{OUTA, B}$ = 1nF	-	5	8.5	mA
UVLO START Threshold		5.9	6.3	6.6	V
UVLO STOP Threshold		5.3	5.7	6.3	V
Hysteresis		-	0.6	-	V
CURRENT SENSE					
Current Limit Threshold		0.55	0.6	0.65	V
CS to OUT Delay	(Note 4)	-	35	-	ns
CS Sink Current		8	10	-	mA
Input Bias Current		-1	-	1	µA
PULSE WIDTH MODULATOR					
Minimum Duty Cycle	V_{ERRO}R < C_T Offset	-	-	0	%
Maximum Duty Cycle	C_T = 470pF, R_{TD} = 51.1KΩ	-	94	-	%
	C_T = 470pF, R_{TD} = 1.1KΩ (Note 4)	-	99	-	%
V_{ERR} to PWM Comparator Input Gain		-	0.8	-	V/V
CT to PWM Comparator Input Gain	(Note 4)	-	1	-	V/V
SS to PWM Comparator Input Gain	(Note 4)	-	0.8	-	V/V
OSCILLATOR					
Charge Current	T_A = 25°C	143	156	170	µA
R_{TD} Voltage		1.925	2	2.075	V
Discharge Current Gain		45	-	65	µA/µA

Electrical Specifications 电气规范 Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block Diagram and Typical Application Schematic. $9V<V_{DD}<16V$, R_{TD}= 51.1KΩ, C_T = 470pF, T_A = -40°C to 105°C (Note 4), Typical values are at T_A= 25°C. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
C_T Valley Voltage		0.75	0.8	0.85	V
C_T Peak Voltage		2.70	2.80	2.90	V
SOFT-START					
Net Charging Current		45	-	68	µA
SS Clamp Voltage		3.8	4.0	4.2	V
Overcurrent Shutdown Threshold Voltage	(Note 4)	-	3.9	-	V
Overcurrent Discharge Current		12	15	23	µA
Reset Threshold Voltage	(Note 4)	0.25	0.27	0.30	V
OUTPUT					
High Level Output Voltage (VOH)	$V_{DD} – V_{OUTA}$ or V_{OUTB}, I_{OUT} = -100mA	-	0.5	2.0	V
Low Level Output Voltage (VOL)	I_{OUT} = 100mA	-	0.5	1.0	V
Rise Time	C_{GATE} = 1nF, V_{DD} = 12V	-	17	60	ns
Fall Time	C_{GATE} = 1nF, V_{DD} = 12V	-	20	60	ns
THERMAL PROTECTION					
Thermal Shutdown	(Note 4)	-	145	-	°C
Thermal Shutdown Clear	(Note 4)	-	130	-	°C
Hysteresis, Internal Protection	(Note 4)	-	15	-	°C

NOTES:

3. Specifications at -40°C are guaranteed by design, not production tested.

4. Guaranteed by design, not 100% tested in production.

Typical Performance Curves

典型性能曲线图

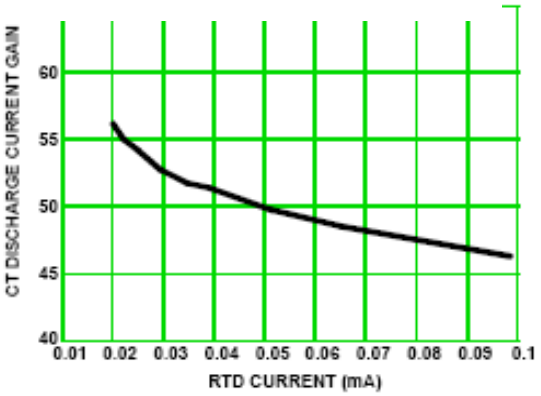


FIGURE 1. OSCILLATOR CT DISCHARGE CURRENT GAIN

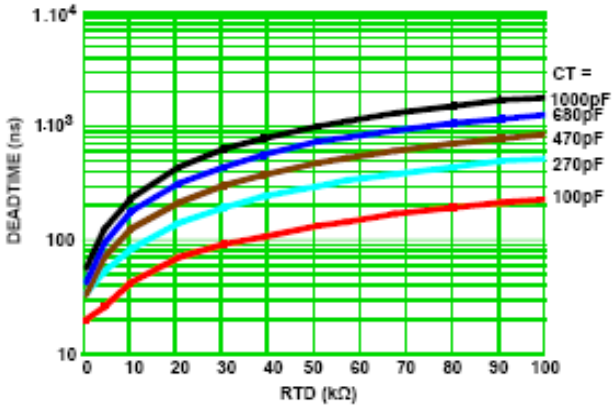


FIGURE 2. DEADTIME vs CAPACITANCE

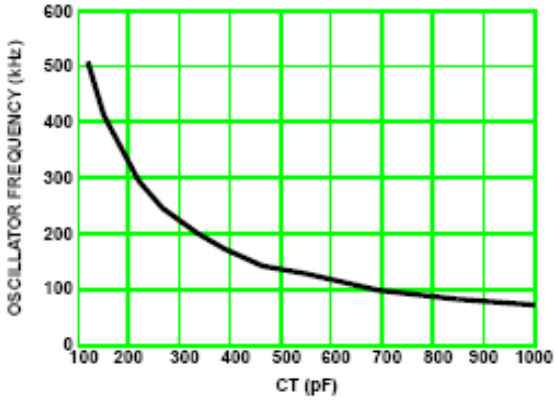


FIGURE 3. CAPACITANCE vs OSCILLATOR FREQUENCY (RTD = 49.9kΩ)

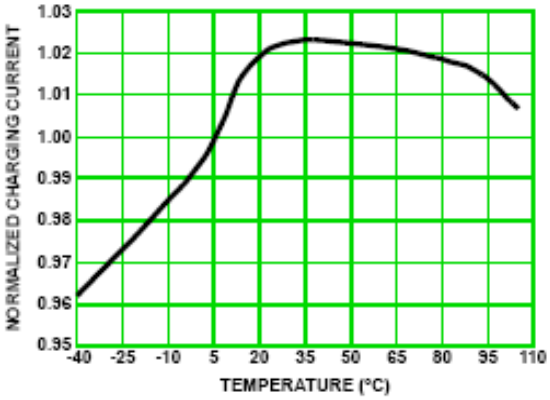


FIGURE 4. CHARGE CURRENT vs TEMPERATURE

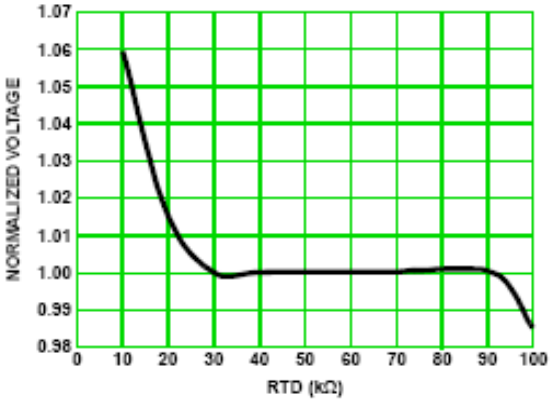


FIGURE 5. TIMING CAPACITOR VOLTAGE vs RTD

ISL6745各管脚简介

V_{DD}

V_{DD}为电源输入端。要优化抗扰度，用一个陶瓷电容器尽可能靠近并挎接在V_{DD}和GND引脚。

IC总供应电流，I_{DD}，取决于OUTA和OUTB输出端的负载。I_{DD}电流是 静态电流和平均输出电流的总和。平均输出电流(I_{OUT})与操工作频率(F_{SW})和每输出端的负载电容的电荷量(Q)成正比，其值可用下式 计 算:

$$I_{OUT} = 2 \times Q \times F_{SW} \quad \text{(EQ. 1)}$$

R_{TD}

这是振荡器定时电容放电电流控制引脚。一个电阻器应连接在这引脚和GND之间。而流经这个电阻的电流决定放电电流的大小。放电电流的通常值则是这电流的55倍。PWM死区时间由定时电容放电时间决定。

C_T

振荡器定时电容应连接在这引脚和GND之 间。

CS

这是过流保护比较器的输入端。过流比较器门限值设置为典型值0.600V。在每个开关周期的末端，CS引脚短接于GND。根据电流传感源阻抗，由于内部时钟和外部电力开关间的延迟，可能要求串联一个电阻。

超出过流门限值会启动延迟关断程序。一旦检测出过流情况，软启动充电电流源就会被截止。而软启动电容通过15μA电流源放电，如果软启动电压降至于3.9V(可承受的过流门限值) 关断条件出现，OUTA和OUTB输出会强制降低。当软启动电压降至0.27V(重新设置门限值)，一个新软启动周期开始。

如果过流情况中断，且在50μs时间内未达到关断门限值（3.9V），过流关断是不会发生。软启动充电电流重新运行且软启动电压复位。

GND

器件上所有功能和电源地都以这个引脚为基准。由于高峰值电流和高频工作，布局必须是低阻抗的。故建议使用地线板块和短接线。

OUTA and OUTB

OUTA 和 OUTB 为交替半周期输出端。每个输出具有 1A 峰值电流的输出能力可驱动 MOSFETs 或 MOSFET 驱动器，且以非常低的阻抗降低过冲和下冲。

SS

在这个引脚与 GND 之间连接软启动定时电容器来控制软启动的时间。电容值决定启动时占空比的增长率，且控制过流关断延迟和过流与短路间歇再启动周期。

功能概述

主要特点

ISL6745 为那些以低成本的桥型拓扑结构且要求准确频率和死区时间控制的应用提供了一个极佳的选择。它有很多特点，其中有 1AFET 驱动器、可调软启动、过流保护和内部过热保护，因而 ISL6745 能以最少量的外部元件做出一个高度灵活的设计。

振荡器

ISL6745通过改变电阻R_{TD}和电容C_T来调振荡器频率高达2MHz。开关周期是定时电容充电和放电时间之和。充电时间由C_T和内部电流源(在式中采用160μA)决定，而放电时间取决于R_{TD} 和C_T。

$$T_C \approx 1.25 \times 10^4 \bullet C_T \quad s \quad \text{(EQ.2)}$$

$$T_D \approx \frac{1}{CTDischargeCurrentGain} \bullet R_{TD} \bullet C_T \quad s \quad \text{(EQ. 3)}$$

$$T_{OSC} = T_C + T_D = \frac{1}{F_{OSC}} \quad s \quad \text{(EQ. 4)}$$

T_C和T_D分别是大概的充电和放电时间，T_{OSC}是振荡器自由运行周期，而F_{OSC}是振荡器频率。放电电流增益(DischargeCurrentGain=45 to 65)可在第3页的表(或Figure1)找到。一个输出的开关周期等于二个振荡器周期。由于传输延迟约5ns，实际 时间比所计算的时间稍微长。这个延迟直接增加到开关时间，且引起定时电容峰值和谷电压门限过冲，因而增大了定时电容峰-峰的电压。另外，如果使用非常低充电和 放电电流， 时间误差将会因C_T引脚处的输入阻抗而增加。

EQ.2至4可帮助估计振荡器频率。在实际上，寄生电部的C_T电容，R_{TD}电压的变化和充电电流遍及温度的变化及其他变化是不可被忽视的。这些对频率的影响最好在真的电路板里评价。EQ. 2依据于基本的电容电流公式，I=C*dV/dt。根据R_{TD}电压的变化(如图4)和充电电流变化(如图5)，公式2的结果将会不同计算出的结果。典型性能曲线和上述的公式一起更精确地估计工作频率。

最大占空比（D_{MAX}）和死区时间（D_T）可用以下公式计算：

$$D_{MAX} = T_C / T_{OSC} \quad \text{(EQ. 5)}$$

$$D_T = T_{OSC} \times (1 - D_{MAX}) \quad \text{(EQ. 6)}$$

软启动运作

ISL6745使用外部电容和内部电流电源来作软启动。软启动降低启动期间的电压和浪涌电流。

在用以驱动 PWM 门控的软启动比较器里，振荡器电容 C_T 信号与软启动 SS 电压作比较。当软启动电压（SS）少于 2.8V 时，占空比会受到限制。输出脉宽随着软启动电容电压的增加而增加。这使软启动期间的占空比可从零增加到最大脉宽。当软启动电压超过 2.8V，软启动完成。软启动开始于起动或因过流关断而复位时。 软启动电压被钳位在 4V.

门极驱动器

ISL6745可灌出和吸收1A峰值电流，且可连接一个MOSFET驱动器如ISL6700作电平转移之用。如要限制峰值电流通过IC，一个外部电阻应连接在IC的推拉输出(OUTA或OUTB引脚)和 MOSFET的门极之间。而这个小串联电阻能阻尼由线组寄生 电感和FET的输入电容的共振所产生的振荡。

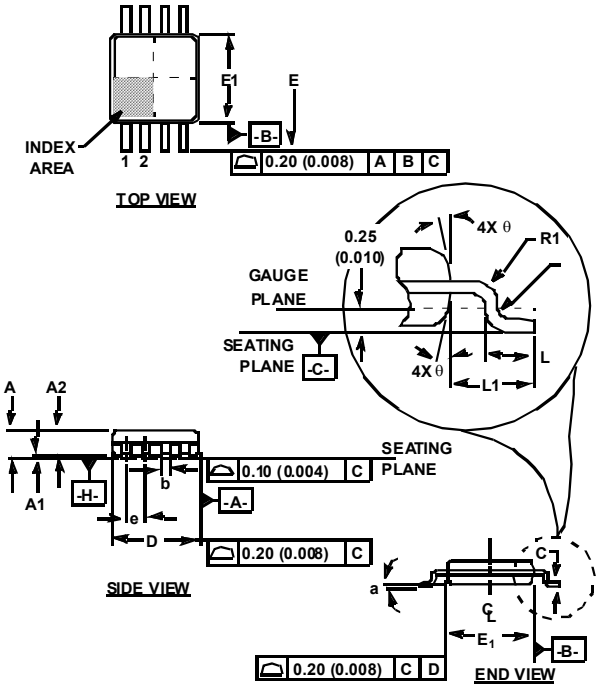
过流运作

软启动周期完成后，过流延迟关断保护才启动。如果检测出过流情况，软启动充电电流电源就会中止，且软启动电容通过15μA电源放电。过流情况停止后，在50μs时间内，如果软启动电容器放电至3.9V，输出停止。这种状态持续到软启动电压降至270mV，开始新软启动周期。如果在软启动电压降至的3.9V前，且过流情况停止至少50μs，软启动充电电流会恢复正常运作，而软启动电压会复位。

过热保护

内热传感器保护器件芯片结温不超出145°C，而热迟滞约15°C。

Mini Small Outline Plastic Packages (MSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums -A- and -B-to be determined at Datum plane -H- .
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

M10.118 (JEDEC MO-187BA)

10 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	
α	0^o	6^o	0^o	6^o	-

Rev.0 12/02